AT73C240-EK1 Evaluation Kit

.....

User Guide





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Introduction

Congratulations on your purchase of the AT73C240-EK1. It is designed to give designers a quick start to evaluate the audio capability of the AT73C240 and for prototyping and testing of new designs.

1.1 Scope

This document describes the AT73C240-EK1. This board is designed to allow an easy evaluation of the products using demonstration software.

To increase its capabilities for demonstration, this standalone board has two serial interfaces (Serial Peripheral Interface and I²S via a dedicated connector).

This user guide acts as a general getting started guide as well as a complete technical reference for advanced users.

This document refers the AT73C240 Datasheet.

Typical Applications:

- MP3-Player
- PDA, Camera, Mobile Phone
- Car Audio/Multimedia
- Home Audio/Multimedia

1.2 AT73C240-EK1 Features

The AT73C240-EK1 provides the following features:

- Power supply:
 - AC/DC transformer input (6V to 9V)
 - or External Power Supply pad
- On-board resources:
 - 20-bit stereo audio DAC,
 - 90dB SNR playback stereo channels,
 - 1 stereo 32 Ohm/20mW stereo headset (3.5mm jack connector),
 - 1 speaker 8 Ohms output (3.5mm jack connector),
 - 1 line stereo input (2 RCA)
- Serial interfaces:
 - SPI (by default),
 - TWI (by hardware modification),
 - l²S
- On-board buttons:
 - AT73C240 Reset,
 - SPI/TWI Communication,
 - TWI Address selection

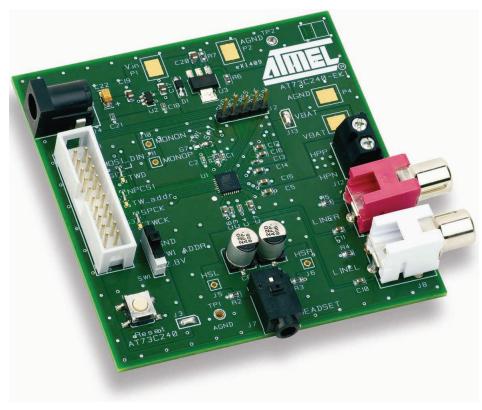
1.3 **Deliverables**

The AT73C240-EK1 package contains the following items:

- An AT73C240-EK1 board,
- A Parallel-to-Serial board,
- A DC/DC power supply cable,
- 20-Lead flat cable,
- A parallel cable,
- One CD-ROM containing the product's software, User Guide and a full Datasheet.



Figure 1-1. AT73C240-EK1 Top View (card photo)



The AT73C240 is located in the center of the AT73C240-EK1 on the Components Side.

Figure 1-2. AT73C240-EK1Card With Available Connections

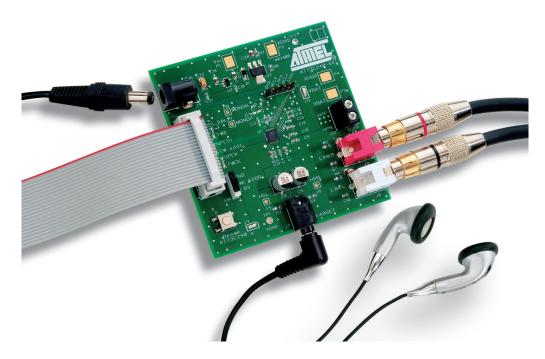
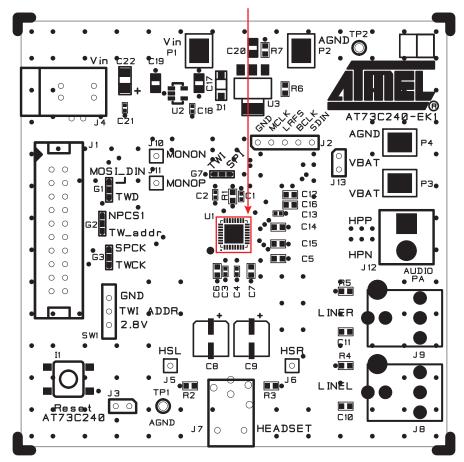




Figure 1-3. AT73C240-EK1 Components Side







Section 2

Getting Started

2.1 Electrostatic Warning

The AT73C240-EK1 evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be connected when handling the board. Avoid touching the components pins or any metallic element.

2.2 Requirements

In order to set up the AT73C240-EK1 evaluation kit the following items are needed:

- 1. The AT73C240-EK1 evaluation board itself.
- 2. A DC output power source for main supply:
 - Transformer 6V to 9V DC max (minimum 500 mA is required) or,
 - External power supply connected to Vin pad.
- 3. A DC output power source for Power Amplifier supply:
 - Transformer 3V to 5.5V DC max (minimum 300mA is required) or,
 - External power supply connected to Vbat pad.
- 4. Input/Output devices (Headset, Speaker, etc)
- 5. PC station with an extension peripheral of SPI/TWI (i.e. Parallel-to-Serial board) for command communication (via micro-controller or PC) and/or an I²S extension for audio streaming.

2.3 PC System Requirements

For a correct software operation of the AT73C240-EK1 evaluation board, the minimum hardware and software PC requirements are:

- Intel[®] Pentium[®] II processor
- 64 MB RAM
- 70 MB free hard disk space (for AT73C240 Evaluation board software installation)
- Windows[®] 2000/XP/VISTA
- A parallel port.

2.4 Instructions

2.4.1 To start the AT73C240-EK1 board (before using the AT73C240-EK1 software)

- Install «DLPORTIO.exe» from the provided software CD and restart your PC.
- Install the AT73C240 software by clicking on setup.exe.
- If the software is downloaded from the Atmel Web site then it is necessary to install first the National Instrument Labview software (LabVIEW8.0.1RuntimeEngine).
- Configure the on-board jumpers as in the relevant paragraphs:
 - 1. Section 2.7.3 "On Board Supply Voltage" on page 2-6
 - 2. Section 2.8.2 "SPI Setup" on page 2-8
 - 3. Section 2.8.3 "TWI Setup" on page 2-9
- Connect DC/DC power supply cable between AT73C240-EK1 board and Parallel-to-Serial card (Section 2.7.1 "AC/DC Transformer or External Power Supply" on page 2-4) or if used connect an external power supply on Audio Amplifier (Section 2.7.2 "Supply With a Power Supply on Audio Power Amplifier" on page 2-6)
- Connect Input and Output devices to the AT73C240-EK1 board (into linein, Headset, Power Amplifier, etc..) as in Section 2.9 "Audio Interfaces" on page 2-11,
- Connect a transformer to the Parallel-to-Serial card,
- Connect the Parallel cable to the Parallel-to-Serial card and then, connect the 20-pin flat cable between the to Parallel-to-Serial card and the AT73C240-EK1 board.
- An I²S serial interface extension (J2) is available for connecting a micro-controller directly to the AT73C240,
- Launch the AT73C240 software Test interface by clicking on AT73C240.exe

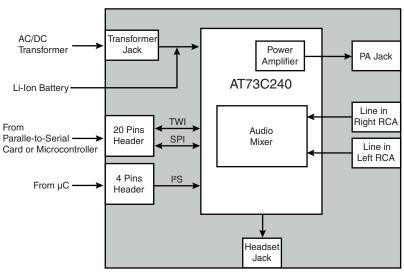
2.4.2 To turn off the AT73C240-EK1 evaluation board

Disconnect the chosen power supply.



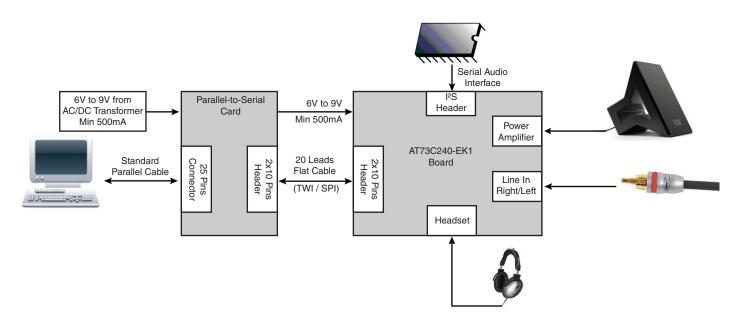
2.5 Block Diagram

Figure 2-1. AT73C240-EK1 Block Diagram



2.6 Typical Connection Application







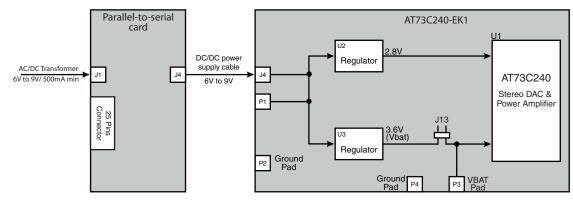
2.7 Power Supply

The AT73C240-EK1 is supplied with the following voltage sources:

- DC/DC Power supply cable from Parallel-to-serial card (connected on J4 of Parallel-to-Serial card and on J4 of AT73C240-EK1) and,
- External Power Supply (connected on J1 of Parallel-to-Serial card) and,
- External Power Supply (connected on P3 of AT73C240-EK1);

This last power supply is not necessary if J13 is closed.

Figure 2-3. Power Supply Diagram



2.7.1 AC/DC Transformer or External Power Supply

The transformer is used as the main power source (Vin) for the AT73C240-EK1. Connect it, to J1 of Parallel-to-serial card (NEB21R type), when using the software.

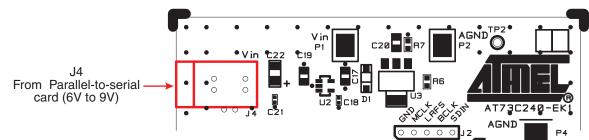
Table 2-1. Transformer Requirements

Power supply source	Min	Мах	Unit
Transformer (minimum 500 mA is required)	6	9	V

The power supply voltage is regulated with on board circuitry. Input voltage on this connector should be between 6V and 9V.

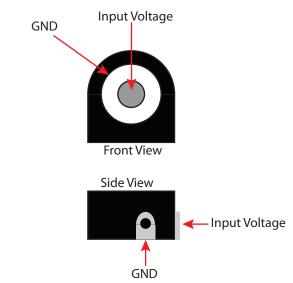
Note: This power supply input is NOT protected against polarization inversion.

Figure 2-4. Operating The AT73C240-EK1(J4)

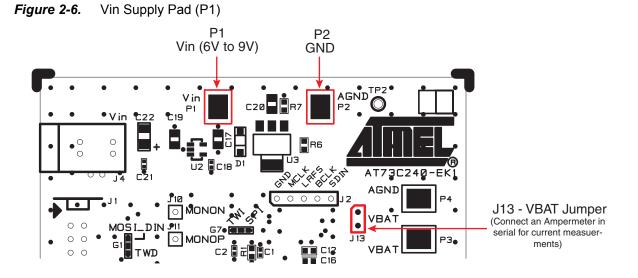








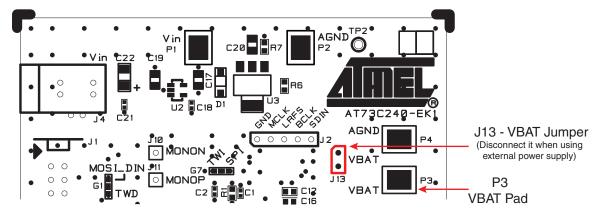
If chosen as an alternative, connect the power supply (+) to Vin pad (P1) and (-) to GND pad (P2).

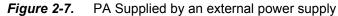




2.7.2 Supply With a Power Supply on Audio Power Amplifier

If chosen, the Audio Power Amplifier of the AT73C240 can be supply by an external supply. Connect the supply (+) to pad P3 and (-) to GND pad P4 and remove the jumper J13.

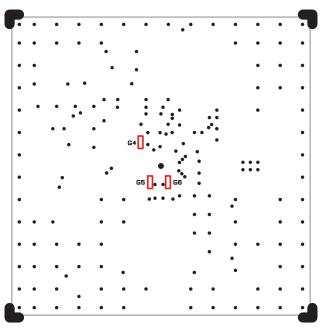




2.7.3 On Board Supply Voltage

The on board supply voltage "grain-cafe" (G4, G5, & G6 located on the print-side of the board - layer 2) enable correct connection between the Power Supply and the AT73C240. Keep these jumpers closed or open them for current measurements (see Figure 2-18 on page 2-13).







2.8 Communication Interfaces

2.8.1 Serial Interfaces Header

The following table details the pin assignments for each signal. In the case of not using the Parallel-to-Serial board, a serial communication (SPI or TWI) cable can drive directly by connecting it to the 2x10 pin header (J1 - Type HE10 for flat cable).

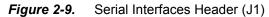
Note: MCLK must run during any SPI or TWI write access. In any case of <u>not using</u> the Serial Board and connecting an external communication system for SPI or TWI, a MCLK should be connected on pin 12. Otherwise, when using the Serial Board, MCLK is provided. Please consult the product Datasheet for MCLK configuration.

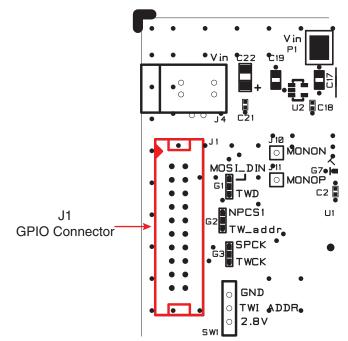
Pin N°	Signal Name	Description	Pin N°	Signal Name	Description
1	MOSI_DIN	Data in	2	-	Not Used
3	SPCK	SPI Clock	4	GND	Ground
5	NPCS1	SPI CS	6	-	Not Used
7	-	Not Used	8	GND	Ground
9	TWCK	TWI Clock	10	2V8	2.8V out
11	LRFS	I ² S LRFS ⁽¹⁾	12	MCLK	I ² S M-clock
13	SDIN	I ² S Data in ⁽¹⁾	14	-	Not Used
15	-	Not Used	16	-	Not Used
17	BCLK	I ² S B-clock ⁽¹⁾	18	SPI_DOUT_MISO	SPI Data out
19	-	Not Used	20	TWD	TWI Data

Table 2-2. Serial Interface Header Pins Assigning

Note: **1.** The I²S signals are independent. They are connected to the Serial Interface Header but not to the level-shifter on the Parallel-to-Serial card.





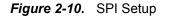


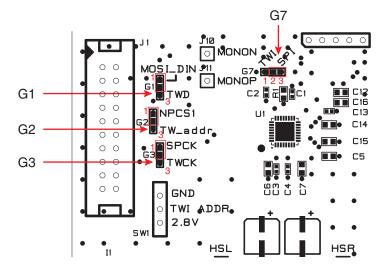
2.8.2 SPI Setup

The SPI protocol is detailed in the product Datasheet.

Before connecting a SPI signal to the Serial Interface Header, configure G1, G2, G3 and G7 as in the following figure (for soldering instructions see Figure 2-19 on page 2-13):

- G1, G2, G3 pads 1 and 2 are soldered
- G7 pads 2 and 3 are soldered





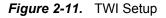


2.8.3 TWI Setup

The TWI protocol is details in the product Datasheet.

Before connecting a TWI signal to the Serial Interface Header, configure G1, G2, G3, G7 and SW1 (for TWI address) as in the following figures (for soldering instructions see Figure 2-19 on page 2-13):

- SW1 is switched to the address when: GND = Address 0x1A and 2.8V = Address 0x1B,
- G1, G2, G3 pads 2 and 3 are soldered,
- G7 pads 1 and 2 are soldered.



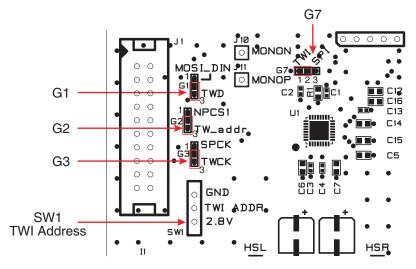


Figure 2-12. TWI Address Switch (SW1) - Case Address = 0

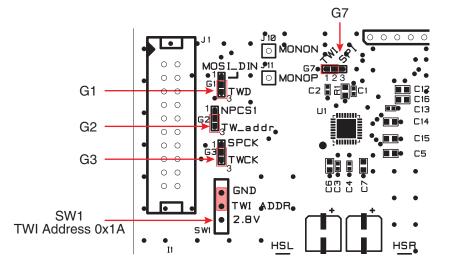
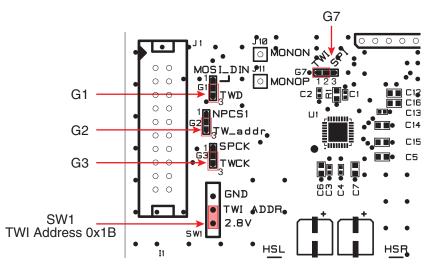




Figure 2-13. TWI Address Switch (SW1) - Case Address = 1



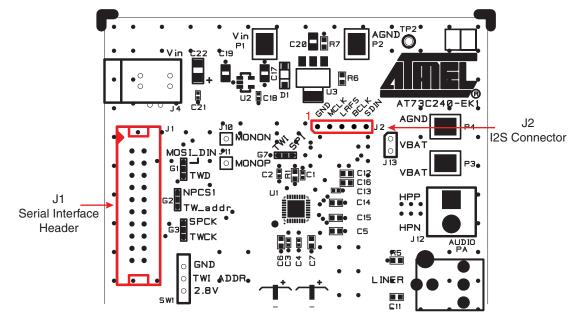
2.8.4 I²S Extension Header

An 1x5 pin header (J2) is use as an extension to directly drive the I²S interface from an external host.

Its signals are connected in Parallel-to-Serial Interface Header (J1). see Section 2-2 "Serial Interface Header Pins Assigning" on page 2-7.

- Pin N° 1 GND.
- Pin N° 2 MCLK.
- Pin N° 3 LRFS.
- Pin N° 4 BCLK.
- Pin N° 5 SDIN.

Figure 2-14. I²S Serial Header (J2)



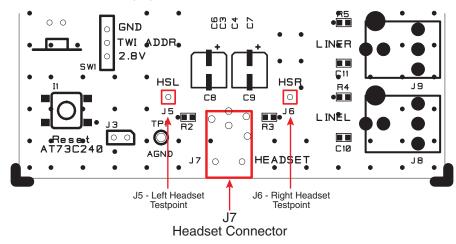


2.9 Audio Interfaces

2.9.1 Headset 32 Ohms Output

The Headset output is connected to a 3.5mm jack connector (J7). The positive and negative output signals can be monitored on J5 and J6.

Figure 2-15. Headset Connector (J7)



2.9.2 Power Amplifier Output (PA)

The Power Amplifier output is connected to a 2-screw connector (J12). The positive output is connected to pin 1 and the negative to pin 2.

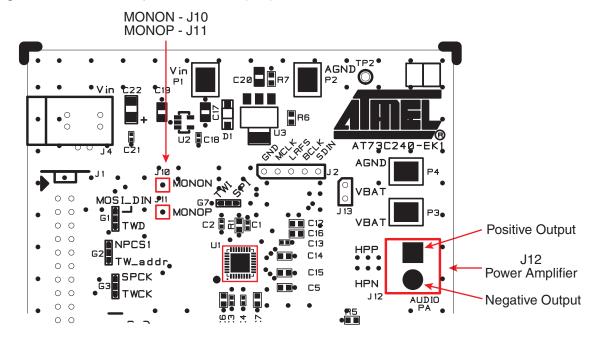


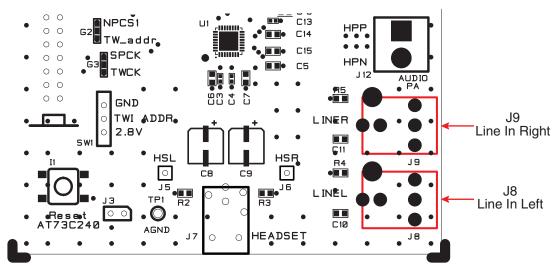
Figure 2-16. Power Amplifier Connector (J12)

Note: By default the MONON and MONOP outputs are looped to PAIN pins (see Figure 7-1 on page 7-1). If needed these signals can be monitored on J10 and J11.

2.9.2.1 Line Inputs

A line stereo signal can be sent through RCA connectors J8 (Left) and J9 (Right).



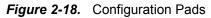


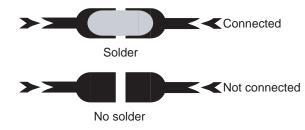


2.10 General Configuration

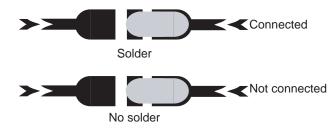
2.10.1 Configuration Pads

A configuration pad configures the AT73C240-EK1 Evaluation Board for custom application. The configuration is programmable by soldering a specific part of the configuration pad. To return to the initial configuration, the customer has to solder a short jumper.









2.10.1.1 Measurement Probing

Any measurement should be done with a CLOSED configuration pad.

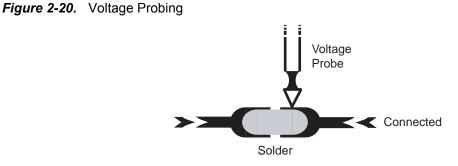
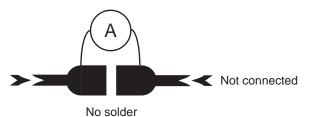


Figure 2-21. Current Probing







Parallel-to-serial Card

The Parallel-to-Serial card allows computer terminals to communicate with all PMAAC product line.

It gives designers all necessary for a quick setup of an extended card and it supports different product's software.

To increase its capabilities for demonstration, this standalone board has two serial interfaces (TWI and SPI).

3.1 Parallel-to-serial Card Features

The Parallel-to-Serial card provides the following features:

- Power supply:
 - AC/DC transformer or,
 - External supply.
- On-board resources:
 - Standard 25 pins Parallel interface,
 - 20 leads GPIO connector,
 - 12.288MHz Clock output for digital core,
 - Adjustable 1.8V to 3.9V output voltage (1A max)
 - Fixed 3.3V output voltage (100mA max),
 - 3 power identification leds.
- Serial interfaces:
 - Bidirectional buffered Parallel to SPI,
 - Bidirectional buffered Parallel to TWI.
- On-board buttons:
 - Vpad Selection.

3.2 Parallel-to-serial Card Components Placement

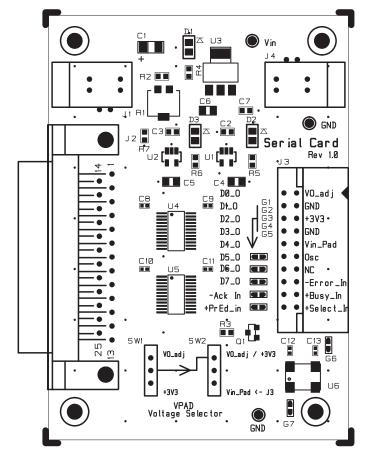


Figure 3-1. Parallel-to-serial Card Components Placement

3.3 Electrostatic Warning

The Parallel-to-Serial card evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be connected when handling the board. Avoid touching the components pins or any metallic element.

3.4 Requirements

In order to set up the Parallel-to-Serial card the following items are needed:

- 4. The Parallel-to-Serial card itself.
- 5. An output DC power source:
 - Transformer 6V to 9V DC max (minimum 500 mA is required) or,
 - External power supply connected to Vin pad.
- 6. PC station with a 25 pins parallel connector.



3.5 Instructions

3.5.1 To start the Parallel-to-Serial card (before using any software)

- Configure the on-board switches and trimmer as in the relevant paragraphs:
 - 1. Section 3.7.2 "Vpad Supply Option" on page 3-7
 - 2. Section 3.7.3 "Adjustable Output Voltage" on page 3-8
 - 3. Section 3.8.2 "12.288 MHz Clock" on page 3-10
 - 4. Section 3.8.3 "On Board Configuration Pads" on page 3-10
 - 5. Section 2.10 "General Configuration" on page 2-13
- Connect a transformer to the Parallel-to-Serial card (Section 3.7.1 "AC/DC Transformer" on page 3-5),
- Connect the Parallel cable to the Parallel-to-Serial card and then,
- Connect the 20-pins flat cable between the to Parallel-to-Serial card and the evaluation board.
- Once the Serial Communication Card properly installed; it should operate transparently as if it were a standard cable connection. Operating power supplied directly from the AC/DC transformer; there is no ON/OFF switch. All data signals from and to the PC are passed straight through.

3.5.2 To turn off the Parallel-to-Serial card evaluation board

Disconnect the chosen power supply.



3.6 Block Diagram

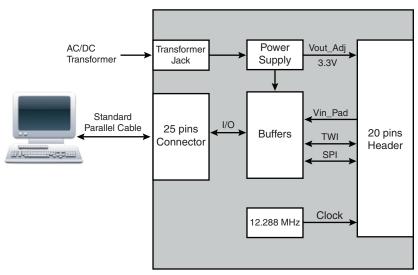
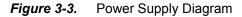


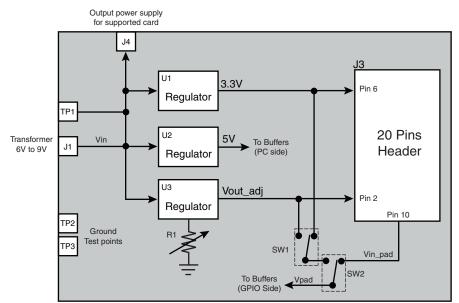
Figure 3-2. Parallel-to-Serial Card Block Diagram

3.7 Power Supply

The Parallel-to-Serial card is supplied with the following voltage sources:

- AC/DC Transformer (connected on J1) or,
- External Power Supply (connected on TP1 and GND)







3.7.1 AC/DC Transformer

The transformer is used as the main power source (AC/DC) for the Parallel-to-Serial card. Connect it, to J1 (NEB21R type), before using any software.

Table 3-1.	Transformer	Requirements
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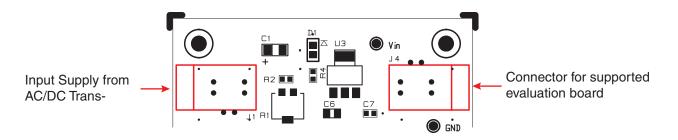
Power supply source	Min	Мах	Unit
Transformer (minimum 500 mA is required)	6	9	V

The power supply voltage is regulated with on board circuitry. Input voltage on this connector should be included between 6V and 9V.

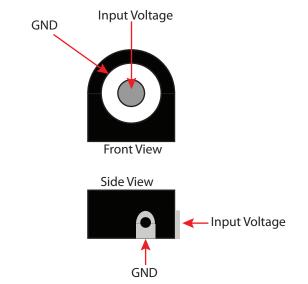
It can supply-power a supported card trough J4 connector which enables to use only the main AC/DC Transformer (connected on J1). Use the two-side male 2.1mm cable to connect power-supply between the two card (see Figure 3-4 on page 3-35).

Note: This power supply input is NOT protected against polarization inversion.





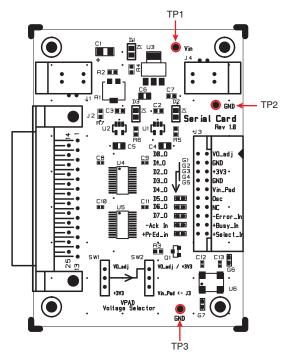




If chosen as an alternative, connect the power supply (+) to Vin test-point (TP1) and (-) to GND tsetpoint(TP2 or TP3).



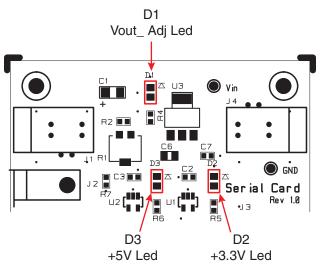
Figure 3-6. Vin Supply Test-Points



On the Parallel-to-Serial card 3 leds indicate voltage present:

- D1 Adjustable Output Voltage
- D2 +3.3V
- D3 +5V





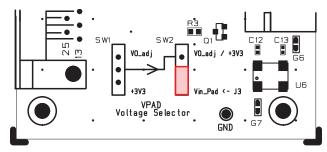


The Vpad is the supply voltage for the buffers for the extension card side. It is the choice of the user to determinate Vpad functionality and there are 3 option:

- 1. Supply by Vin_Pad from an extension card (pin 10 on J3).
- 2. Supply by 3.3V from on board 3.3V LDO (U2)
- 3. Supply by adjustable voltage from on board adjustable Regulator (U3); see "Adjustable Output Voltage" on page 3-8

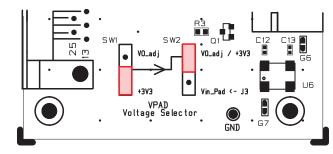
Please consult the following 3 figures for Vpad supply available options.

Figure 3-8. Vpad Supplied By Vin_Pad



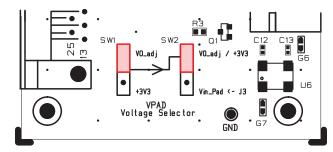
SW2 is in Vin_Pad position. SW1 has no effect.

Figure 3-9. Vpad Supplied By On Board 3.3V



SW2 is in VO_adj/+3V3 position. SW1 is in +3V3 position.

Figure 3-10. Vpad Supplied By Board Adjustable Voltage

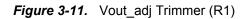


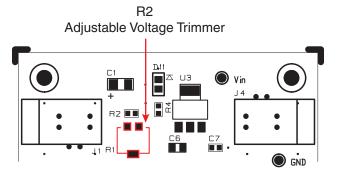
SW2 is in VO_adj/+3V3 position. SW1 is in VO_adj position.



3.7.3 Adjustable Output Voltage

The Parallel-to-Serial card is able to supply up to 1A adjustable output voltage (Vout_adj = 1.8V to 3.9V) for powering an extended card. Vout_adj output level is trimmed by R1 and Its output pin is located on pin N° 2 on J3 header.







3.8 Communication Interfaces

3.8.1 Serial Interfaces Header

The Parallel-to-Serial card supports both SPI and TWI protocols which configured automatically by the software. The following table details the pins assigning for each signal on J3 (2x10 pins header - Type HE10 for flat cable).

Note: In most cases, a clock must run during any SPI or TWI write access. In any case of <u>not using</u> the Serial Board and connecting an external communication system for SPI or TWI a clock should be provided to the supported evaluation card.

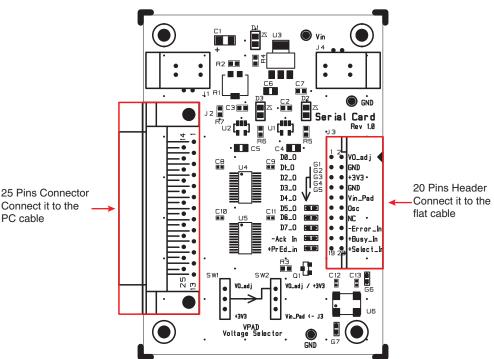
Pin N°	Signal Name	Description	Pin N°	Signal Name	Description
1	Data0_Out	Output Data ⁽¹⁾	2	Vout_adj	Adjustable Output Voltage (1A max) ⁽⁴⁾
3	Data1_Out	Output Data ⁽¹⁾	4	GND	Ground ⁽³⁾
5	Data2_Out	Output Data ⁽¹⁾	6	+3V3	Output voltage (100mA max)
7	Data3_Out	Output Data ⁽¹⁾	8	GND	Ground ⁽³⁾
9	Data4_Out	Output Data ⁽¹⁾	10	Vin_pad	Input supply from supported card
11	Data5_Out	Output Data ⁽¹⁾	12	OSC	12.288MHz Output clock for supported digital core
13	Data6_Out	Output Data ⁽¹⁾	14	NC	Not Connected
15	Data7_Out	Output Data ⁽¹⁾	16	-Error_in	Input Data ⁽²⁾
17	-Ack_in	Input Data ⁽²⁾	18	+Busy_in	Input Data ⁽²⁾
19	+PaperEnd_in	Input Data ⁽²⁾	20	+SelectIn_in	Input Data ⁽²⁾

Table 3-2. Serial Interface Header Pins Assigning

Notes: 1. Output Data - An output signal from parallel port to supported card.

- 2. Input Data An input signal from supported card to parallel port.
- **3.** Ground These pins must be connected between the Parallel-to-Serial card and the supported board.
- 4. Output current is determinate by the limitation of the ACDC transformer.

Figure 3-12. Serial Interfaces Connectors (J2 & J3)

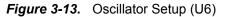


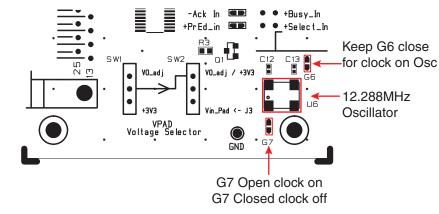
3.8.2 12.288 MHz Clock

The Parallel-to-Serial card's oscillator (X1) provides 12.288MHz clock (+3.3V p-p). This clock is necessary for driving the digital core of the evaluated board - via pin 12 on J3.

G6 connect the oscillator output clock with pin 12 on J3. Open it if clock is not necessary.

Keep G7 enables/disable the oscillator. If open then clock is "ON". If closed then clock is "OFF".





3.8.3 On Board Configuration Pads

The "Grain-cafe" G1 to G5 are **not soldered** by default. Simply solder it if these signal should be connected to the buffers.





AT73C240-EK1 Software Interface

4.1 Software Panel

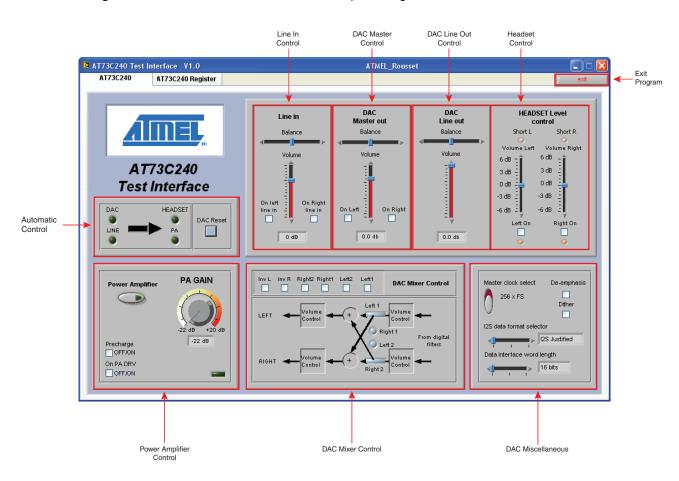
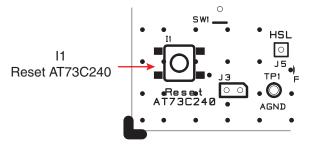


Figure 4-1. Software Panel - General Purpose Page



		(Mu	TWI/SPI Selector ust be setup ore startup)	Read Command	Write Command	i i	Write Content	Read Content		gister dress
	AT73C240 Test Inte	rface V1.0 T73C240 Register			A	TMEL_Rousse	et 🛛			exit
Automatic Readegister Mapping		Read ofFion	Input interfac communicati TVI - SPI - Y TVI Address 0x1B - y	n	Write Read	_	240 7 ite content	rest Int		ddress
		Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	BitO
	0x00 DAC Contro	1		ONPADRV		ONDACL	ONLNOR			DICO
	0x00 DAG CONT	1	1.	ONPADRO	ONDACR	ONDACL	ONLINOK	ONLNOL	ONLNIR	ONLNIL
	0x01 DAC Left Li			-	ONDACR	LLIG	LLIG	ONLNOL	ONLNIR LLIG	
		ne In Gain								ONLNIL
	0x01 DAC Left Li 0x02 DAC Right L 0x03 DAC Left M	ne In Gain ine In Gain aster Playback Gain	-	-	- LMPG	LLIG RLIG LMPG	LLIG RLIG LMPG	LLIG RLIG LMPG	LLIG RLIG LMPG	ONLNIL LLIG RLIG LMPG
	0x01 DAC Left Li 0x02 DAC Right L 0x03 DAC Left M 0x04 DAC Right M	ne In Gain ine In Gain aster Playback Gain flaster Playback Gain	- - -	- - - -	- LMPG RMPG	LLIG RLIG LMPG RMPG	LLIG RLIG LMPG RMPG	LLIG RLIG LMPG RMPG	LLIG RLIG LMPG RMPG	ONLNIL LLIG RLIG LMPG RMPG
	0x01 DAC Left Li 0x02 DAC Right L 0x03 DAC Left M 0x04 DAC Right N 0x05 DAC Left Li	ne In Gain ine In Gain aster Playback Gain flaster Playback Gain ne Out Gain		- - - -	- LMPG RMPG LLOG	LLIG RLIG LMPG RMPG LLOG	LLIG RLIG LMPG RMPG LLOG	LLIG RLIG LMPG RMPG LLOG	LLIG RLIG LMPG RMPG LLOG	ONLNIL LLIG RLIG LMPG RMPG LLOG
	0x01 DAC Left Li 0x02 DAC Right L 0x03 DAC Left M 0x04 DAC Right L 0x05 DAC Left Li 0x06 DAC Right L	ne In Gain ine In Gain aster Playback Gain flaster Playback Gain ne Out Gain ine Out Gain		- - - - -	- LMPG RMPG LLOG RLOG	LLIG RLIG LMPG RMPG LLOG RLOG	LLIG RLIG LMPG RMPG LLOG RLOG	LLIG RLIG LMPG RMPG LLOG RLOG	LLIG RLIG LMPG RMPG LLOG RLOG	ONLNIL LLIG RLIG LMPG RMPG LLOG RLOG
	0x01 DAC Left Li 0x02 DAC Right L 0x03 DAC Left M 0x04 DAC Right L 0x05 DAC Left M 0x05 DAC Left Li 0x06 DAC Right L 0x07 DAC Output	ne In Gain ine In Gain aster Playback Gain Master Playback Gain ne Out Gain ine Out Gain Level Control	RSHORT	- - - - - - ROLC	- LMPG RMPG LLOG RLOG ROLC	LLIG RLIG LMPG RMPG LLOG RLOG ROLC	LLIG RLIG LMPG RMPG LLOG RLOG LSHORT	LLIG RLIG LMPG LLOG RLOG LOLC	LLIG RLIG LMPG RMPG LLOG RLOG LOLC	ONLNIL LLIG RLIG LMPG RMPG LLOG RLOG LOLC
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left M 0x04 DAC Right Li 0x05 DAC Left M 0x06 DAC Right Li 0x06 DAC Right Li 0x06 DAC Right Li 0x07 DAC Night Li 0x08 DAC Night Li	ne In Gain Ine In Gain aster Playback Gain daster Playback Gain ne Out Gain Level Control Control Control		- - - - - - - - - - - - - - - - - - -	- LMPG RMPG LLOG RLOG ROLC INVR	LLIG RLIG LMPG LLOG RLOG RLOG ROLC INVL	LLIG RLIG LMPG LLOG RLOG LSHORT RMSMIN2	LLIG RLIG LMPG LLOG RLOG LOLC RMSMIN1	LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN2	ONLNIL LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN1
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left M 0x04 DAC Right Li 0x05 DAC Right Li 0x06 DAC Right Li 0x07 DAC Cotput 0x08 DAC Output 0x08 DAC Might Li 0x08 DAC Cock -	ne In Gain ine In Gain aster Playback Gain daster Playback Gain ne Out Gain ine Out Gain Level Control Control 3. Sampling Frequency Control	RSHORT	- - - - - ROLC -	- LMPG RMPG LLOG RLOG ROLC INVR	LLIG RLIG LMPG RMPG LLOG RLOG ROLC INVL OVRSEL	LLIG RLIG LMPG LLOG RLOG LSHORT RMSMIN2	LLIG RLIG LMPG LLOG RLOG LOLC RMSMIN1	LLIG RLIG LMPG RMPG LLOG RLOG LOLC LM5MIN2	ONLNIL LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN1
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left Min 0x04 DAC Left Li 0x05 DAC Left Li 0x07 DAC Output 0x08 DAC Mixer 0x08 DAC Mixer 0x09 DAC Colock 0x00A DAC Mixer	ne In Gain Ine In Gain Sater Playback Gain faster Playback Gain ne Out Gain Level Control Level Control 3 Sampling Frequency Control I aneous		- - - - - - - - - - - - - - - - - - -	- LMPG RMPG LLOG RLOG ROLC INVR	LLIG RLIG LMPG RMPG LLOG RLOG ROLC INVL OVRSEL DINTSEL	LLIG RLIG LMPG LLOG RLOG LSHORT RMSMIN2 DITHEN	LLIG RLIG LMPG LLOG RLOG LOLC RMSMIN1 DEEMPEN	LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN2 - NBITS	ONLNIL LLIG RLIG LMPG LMPG LLOG RLOG LOC LMSMINI - NBITS
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left M 0x04 DAC Right Li 0x05 DAC Right Li 0x06 DAC Right Li 0x07 DAC Chight Li 0x08 DAC Right Li 0x08 DAC Night Li 0x08 DAC Night Li 0x08 DAC Chick I	ne In Gain Ine In Gain Sater Playback Gain faster Playback Gain ne Out Gain Level Control Level Control 3 Sampling Frequency Control I aneous			LMPG RMPG LLOG RLOG ROLC INVR DINTSEL	LLIG RLIG LMPG RMPG LLOG RLOG ROLC INVL OVRSEL	LLIG RLIG LMPG LLOG RLOG LSHORT RMSMIN2	LLIG RLIG LMPG LLOG RLOG LOLC RMSMIN1	LLIG RLIG LMPG RMPG LLOG RLOG LOLC LM5MIN2	ONLNIL LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN1
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left M 0x04 DAC Right Li 0x05 DAC Left M 0x06 DAC Right Li 0x06 DAC Right Li 0x06 DAC Right Li 0x07 DAC Color Mixer 0x08 DAC Right Li 0x09 DAC Color Mixer 0x00 DAC Right Li	ne In Gain Ine In Gain Sater Playback Gain 4aster Playback Gain ne Out Gain Ine Out Gain Level Control Control Sampling Frequency Control Ianeous arge Control		ROLC VCMCAPSEL	LMPG RMPG LLOG RLOG ROLC INVR DINTSEL	LLIG RLIG LMPG RMPG LLOG RLOG ROLC INVL OVRSEL DINTSEL PRCHGPDRV	LLIG RLIG LMPG LLOG RLOG LSHORT RMSMIN2 - DITHEN PRCHGLNIR	LLIG RLIG LMPG LLOG RLOG LOLC RMSMINI - DEEMPEN PRCHGLNIL	LLIG RLIG LMPG RMPG LLOG RLOG LOLC LMSMIN2 - NBITS PRCHG	ONLINIL LLIG RLIG LMPG LLOG RLOG LLOLC LMSTINI NBITS ONMSTR
	0x01 DAC Left Li 0x02 DAC Right Li 0x03 DAC Left Ministry 0x04 DAC Right Ministry 0x05 DAC Right Ministry 0x06 DAC Right Ministry 0x06 DAC Right Ministry 0x07 DAC Output 0x08 DAC Right Ministry 0x08 DAC Ministry 0x08 DAC Clock 0x00 DAC Right Ministry 0x00 DAC Ministry 0x00 DAC Right Ministry 0x01 DAC Right Ministry	ne In Gain Ine In Gain Sater Playback Gain 4aster Playback Gain ne Out Gain Ine Out Gain Level Control Control Sampling Frequency Control Ianeous arge Control		- - - ROLC - - VCMCAPSEL -	LMPG RMPG LLOG RLOG ROLC INVR - DINTSEL	LLIG RLIG LMPG RMPG LLOG ROLC INVL OVRSEL DINTSEL PRCHEDRV	LLIG RLIG RMPG LLOG RLOG LSHORT RMSMIN2 DITHEN PRCHGLNIR	LLIG RLIG LMPG LLOG RLOG LOLC RMSMIN1 DEEMPEN PRCHGLNIL	LLIG RLIG LMPG LLOG LLOG LOLC LMSMIN2 NBITS PRCHG RESFILZ	ONLINIL LLIG RLIG LMPG LLOG LLOG LOLC LOLC LMSMINI NBITS ONMSTR RSTZ

- *Note:* Resetting all the registers done by pressing once on the AT73C240 Reset push-button I2. In the next read action the registers will be at their default values.
- Figure 4-3. Reset AT73C240 Button







Section 5

Technical Specifications

5.1 AT73C240-EK1

System Unit: AT73C240-EK1	
 Physical Dimensions Weight 	
 Operating Conditions 	
 External Voltage Supply (From AC/DC Transformer or on Vin Pad) 	6V - 9V /500 mA
 External Voltage Supply (on VBAT Pad) 	3V - 5.5V
Connections	
- Communication Connector	2x10 pins Header
 – I²S Serial Connector 	1x5 pins Header

5.2 Parallel-to-Serial Card

System Unit: Parallel-to-Serial card	
 Physical Dimensions Weight 	
 Operating Conditions 	
 External Voltage Supply (From AC/DC Transformer) 	6V - 9V /500 mA
Connections	
- Communication Connector	2x10 pins Header

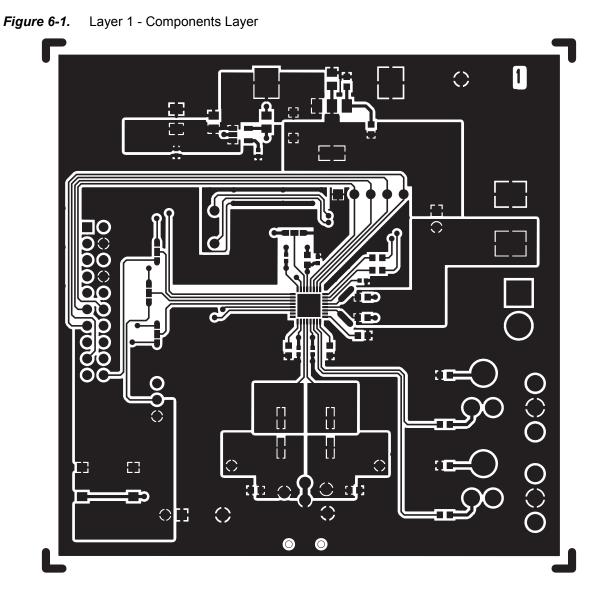


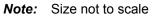


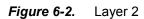
Section 6

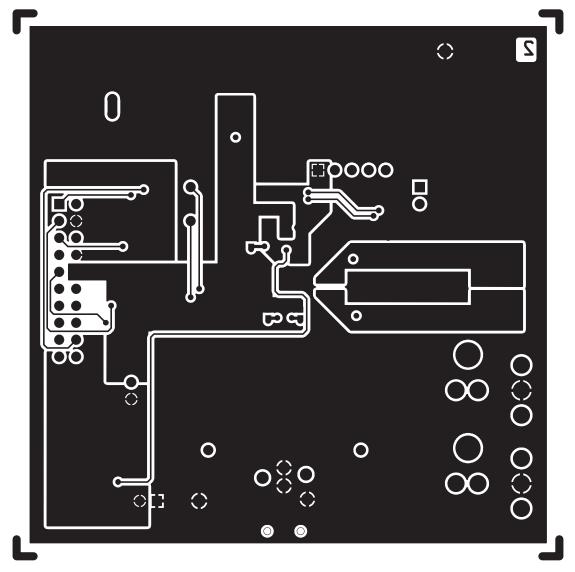
PCB Layout

6.1 AT73C240-EK1







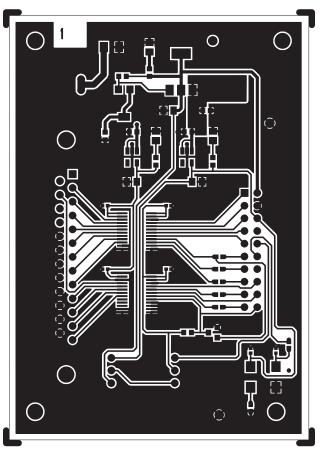


Note: Size not to scale



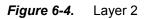
6.2 Parallel-to-Serial Card

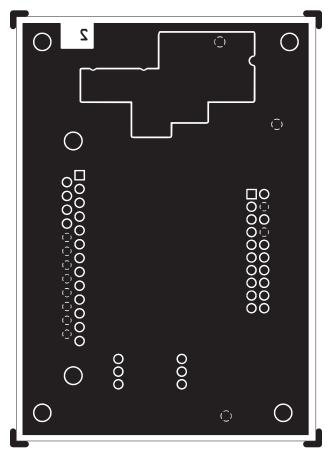
Figure 6-3. Layer 1 - Components Layer



Note: Size not to scale







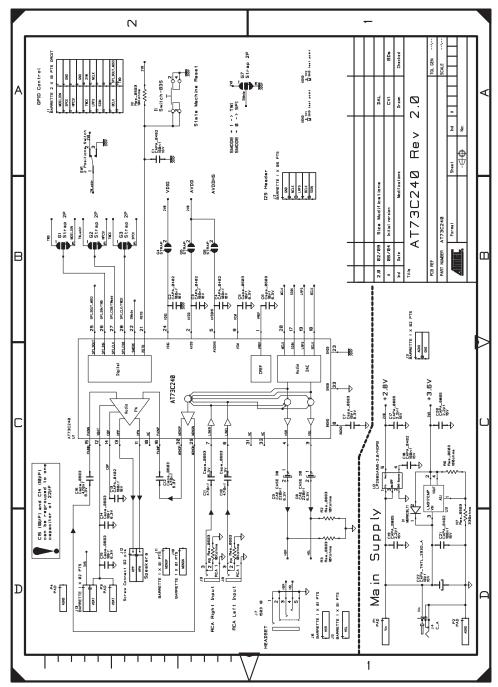
Note: Size not to scale





Schematics

Figure 7-1. AT73C240-EK1 Schematic



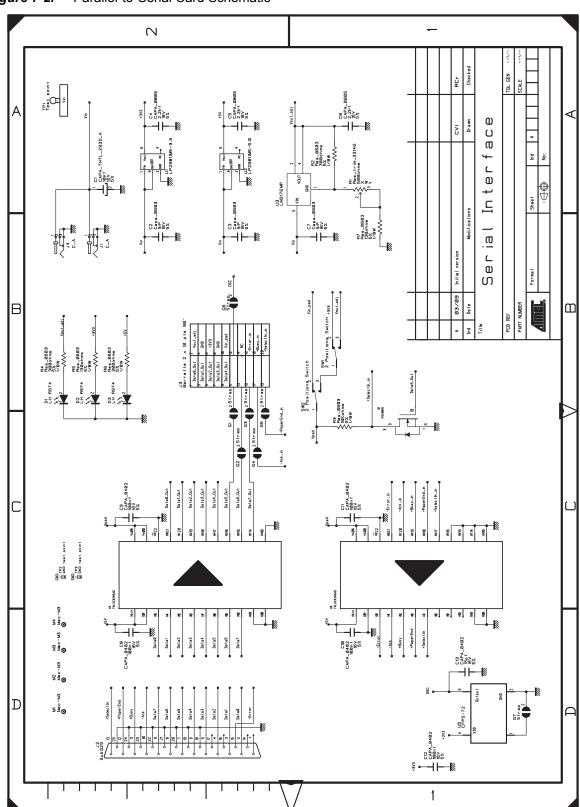


Figure 7-2. Parallel-to-Serial Card Schematic





Section 8

Revision History

8.1 Revision History

Table 8-1. Revision History

Document	Comments	Change Request Ref.
6482A	First Issue, 15-May-2009	





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